ABSTRACT

In one embodiment of the invention, during add-compare-select computations, the output of the adders is guaranteed to be a positive value because the only time normalization logic subtracts a normalization amount is when all accumulators are greater than the normalization amount. As such, the detection of overflow is greatly simplified. Overflow in the add-compare-select unit may be indicated simply by the value of the most significant bit ("MSB") (i.e., the sign bit) of the result. If the MSB of the result of the adder is set then, in one embodiment, the output of the adder gets forced the maximum possible value given the number of bits. For example, this value will be forced to 7h7f if the value is represented by 7-bits. That is to say, if an overflow is detected, then the accumulator is saturated to the maximum value.